AFBR-703SDDZ
10Gb/1Gb Ethernet, 850nm
SFP+ Transceiver

Data Sheet



Description

The Avago AFBR-703SDDZ transceiver is part of a family of SFP+ products. This transceiver utilizes Avago's 850nm VCSEL and PIN Detector technology to provide an IEEE 10Gb Ethernet design compliant with the 10GBASE-SR standard and allows the operation at 1.25GBd for Gigabit Ethernet application. The AFBR-703SDDZ transceiver is designed to enable 10Gb Ethernet equipment designs with very high port density based on the new electrical and mechanical specification enhancements to the well known SFP specifications developed by the SFF Committee. These specifications are referred to as SFP+ to recognize these enhancements to previous SFP specifications used for lower speed products. Avago Technologies is an active participant in the SFF Committee specification development activities.

Related Products

- AFCT-701SDDZ SFP+ 10Gb/1Gb Gigabit Ethernet 10GBASE-LR transceiver for operation in SMF link applications to 10 km
- AFBR-703SDZ (AFBR-703ASDZ) SFP+ 10 Gigabit Ethernet 10GBASE-SR transceiver with case temperature 0-70°C (0-85°C) for use on multimode fiber cables. It is best suited for OM3 high bandwidth MMF link applications with link lengths up to 300 meters.
- AFBR-707SDZ SFP+ 10 Gigabit Ethernet 10GBASE-LRM transceiver for 220 meter operation in all MMF link applications including OM1 and OM2 legacy fiber cables and new high bandwidth OM3 fiber cables.
- AFCT-701SDZ (AFCT-701ASDZ) SFP+ 10 Gigabit Ethernet 10GBASE-LR transceiver with case temperature 0-70°C (0-85°C) for operation in SMF link applications to 10 km
- AFCT-5016Z SFP+ Evaluation Board The purpose of this SFP+ evaluation board is to provide the designer with a convenient means for evaluating SFP+ fiber optic transceivers.

Features

- Avago 850nm VCSEL source and Transmitter Optical Subassembly technology
- Avago PIN detector and Receiver Optical Subassembly technology
- Typical power dissipation 600mW
- Full digital diagnostic management interface
- Avago SFP+ package design enables equipment EMI performance in high port density applications with margin to Class B limits
- Flexibility in data rate selection through either hardware or software control

Specifications

- Optical interface specifications per IEEE 802.3ae 10GBASE-SR
- Compliant to the transmitter extinction ratio and the receiver sensitivity specs per IEEE 802.3 Gigabit Ethernet (1.25GBd) 1000BASE-SX
- Electrical interface specifications per SFF Committee SFF 8431 Specifications for Enhanced 8.5 and 10 Gigabit Small Form Factor Pluggable Module "SFP+"
- Management interface specifications per SFF Committee SFF 8431 and SFF 8472 Diagnostic Monitoring Interface for Optical Transceivers
- Mechanical specifications per SFF Committee SFF 8432 Improved Pluggable Formfactor "IPF"
- LC Duplex optical connector interface confirming to ANSI TIA/EA 604-10 (FOCIS 10A)
- Compliant to Restriction on Hazardous Substances (RoHS) per EU and China requirements
- Compliant to halogen free requirements
- Class 1 Eye safe per requirements of IEC 60825-1 / CDRH

Patent - www.avagotech.com/patents

Description, continued

Installation

The AFBR-703SDDZ transceiver package is compliant with the SFF 8432 Improved Pluggable Formfactor housing specification for the SFP+. It can be installed in any INF-8074 or SFF-8431/2 compliant Small Form Pluggable (SFP) port regardless of host equipment operating status The AFBR-703SDDZ is hot-pluggable, allowing the module to be installed while the host system is operating and on-line. Upon insertion, the transceiver housing makes initial contact with the host board SFP cage, mitigating potential damage due to Electro-Static Discharge (ESD).

By selecting TX rate select to 1.25 Gbps operation, the module TX performance complies with the extinction ratio and output power level in 1000BASE-SX specifications.

Likewise RX performance complies with the sensitivity performance in the 1000BASE-SX specifications by selecting RX rate select to 1.25 Gbps operation.

The rate select can be done through either the hardware pins or the software access to the A2h page of EEPROM map. The user can refer to the Appendix for details of rate select.

Digital Diagnostic Interface and Serial Identification

The two-wire interface protocol and signaling detail are based on SFF-8431. Conventional EEPROM memory, bytes 0-255 at memory address 0xA0, is organized in compliance with SFF-8431. New digital diagnostic information, bytes 0-255 at memory address 0xA2, is compliant to SFF-8472. The new diagnostic information provides the opportunity for Predictive Failure Identification, Compliance Prediction, Fault Isolation and Component Monitoring.

Predictive Failure Identification

The AFBR-703SDDZ predictive failure feature allows a host to identify potential link problems before system performance is impacted. Prior identification of link problems enables a host to service an application via "fail over" to a redundant link or replace a suspect device, maintaining system uptime in the process. For applications where ultra-high system uptime is required, a digital SFP provides a means to monitor two real-time laser metrics associated with laser degradation and predicting failure: average laser bias current (Tx_Bias) and average laser optical power (Tx_Power).

Compliance Prediction

Compliance prediction is the ability to determine if an optical transceiver is operating within its operating and environmental requirements. AFBR-703SDDZ devices provide real-time access to transceiver internal supply voltage and temperature, allowing a host to identify potential component compliance issues. Received optical power is also available to assess compliance of a cable plant and remote transmitter. When operating out of requirements, the link cannot guarantee error free transmission.

Fault Isolation

The fault isolation feature allows a host to quickly pinpoint the location of a link failure, minimizing downtime. For optical links, the ability to identify a fault at a local device, remote device or cable plant is crucial to speeding service of an installation. AFBR-703SDDZ real-time monitors of Tx_Bias, Tx_Power, Vcc, Temperature and Rx_Power can be used to assess local transceiver current operating conditions. In addition, status flags TX_DISABLE and Rx Loss of Signal (LOS) are mirrored in memory and available via the two-wire serial interface.

Component Monitoring

Component evaluation is a more casual use of the AFBR-703SDDZ real-time monitors of Tx_Bias, Tx_Power, Vcc, Temperature and Rx_Power. Potential uses are as debugging aids for system installation and design, and transceiver parametric evaluation for factory or field qualification. For example, temperature per module can be observed in high density applications to facilitate thermal evaluation of blades, PCI cards and systems.

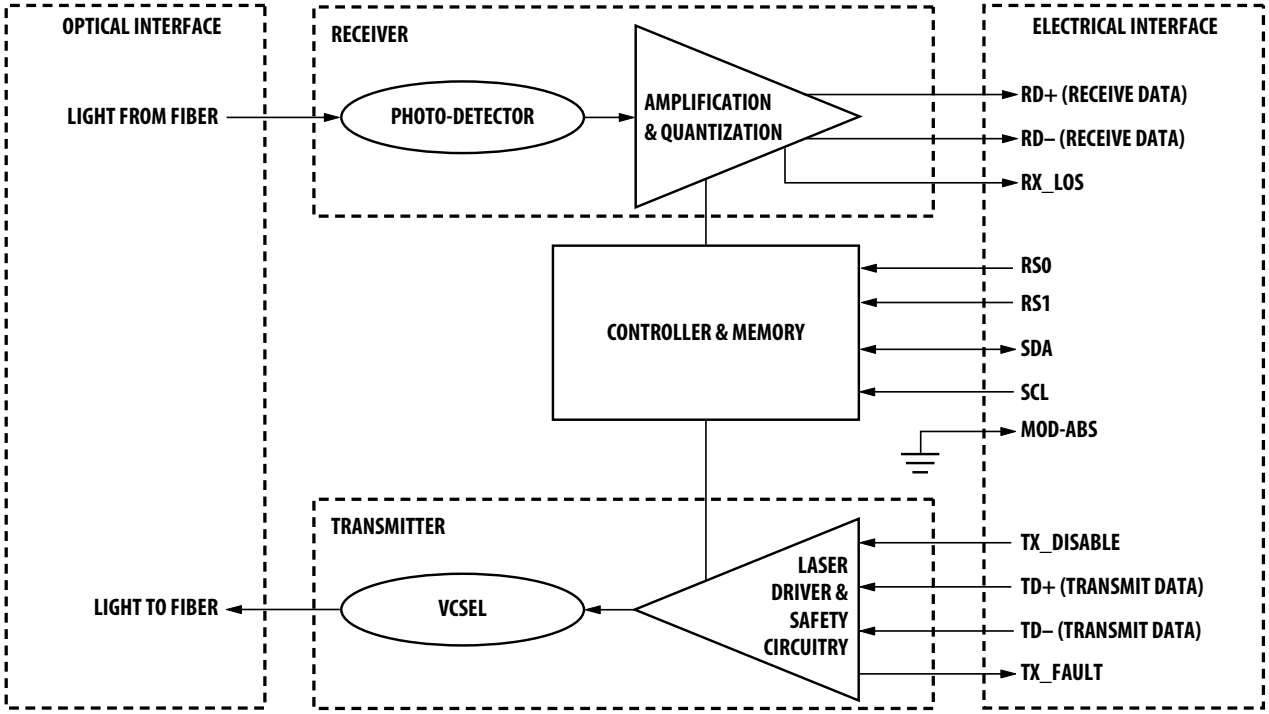


Figure 1. Transceiver functional diagram

Transmitter Section

The transmitter section includes the Transmitter Optical Sub-Assembly (TOSA) and laser driver circuitry. The TOSA, containing an Avago designed and manufactured 850 nm VCSEL (Vertical Cavity Surface Emitting Laser) light source, is located at the optical interface and mates with the LC optical connector. The TOSA is driven by an IC which uses the incoming differential high speed logic signal to modulate the laser diode driver current. This Tx laser driver circuit regulates the optical power at a constant level provided the incoming data pattern is DC balanced.

Transmit Disable (TX_DISABLE)

The AFBR-703SDDZ accepts an LVTTL compatible transmit disable control signal input which shuts down the transmitter optical output. A high signal implements this function while a low signal allows normal transceiver operation. In the event of a fault (e.g. eye safety circuit activated), cycling this control signal resets the module as depicted in Figure 6. An internal pull up resistor disables the transceiver transmitter until the host pulls the input low. TX_DISABLE can also be asserted via the two-wire interface (address A2h, byte 110, bit 6) and monitored (address A2h, byte 110, bit 7).

The contents of A2h, byte 110, bit 6 are logic OR'd with hardware TX_DISABLE (contact 3) to control transmitter operation.

Transmit Fault (TX_FAULT)

A catastrophic laser fault will activate the transmitter signal, TX_FAULT, and disable the laser. This signal is an open collector output (pull-up required on the host board). A low signal indicates normal laser operation and a high signal indicates a fault. The TX_FAULT will be latched high when a laser fault occurs and is cleared by toggling the TX_DISABLE input or power cycling the transceiver. The transmitter fault condition can also be monitored via the two-wire serial interface (address A2, byte 110, bit 2).

Receiver Section

The receiver section includes the Receiver Optical Sub-Assembly (ROSA) and the amplification/quantization circuitry. The ROSA, containing a PIN photodiode and custom transimpedance amplifier, is located at the optical interface and mates with the LC optical connector. The ROSA output is fed to a custom IC that provides post-amplification and quantization.

Receiver Loss of Signal (Rx_LOS)

The post-amp IC also includes transition detection circuitry which monitors the AC level of incoming optical signals and provides a LVTTL/CMOS compatible status signal to the host. A high status signal indicates loss of modulated signal, indicating link failures such as broken fiber or failed transmitter. Rx_LOS can also be monitored via the two-wire serial interface (address A2h, byte 110, bit 1).

Functional Data I/O

The AFBR-703SDDZ interfaces with the host circuit board through the twenty contact SFP+ electrical connector. See Table 2 for contact descriptions. The module edge connector is shown in Figure 4. The host board layout for this interface is depicted in Figure 7.

The AFBR-703SDDZ high speed transmit and receive interfaces require SFF-8431 compliant signal lines on the host board. To simplify board requirements, biasing resistors and AC coupling capacitors are incorporated into the SFP+ transceiver module (per SFF-8431) and hence are not required on the host board. The TX_DISABLE, TX_FAULT and RX_LOS signals require LVTTL signals on the host board (per SFF-8431) if used. If an application does not take advantage of these functions, care must be taken to ground TX_DISABLE to enable normal operation.

Figure 2 depicts the recommended interface circuit to link the AFBR-703SDDZ to supporting physical layer ICs. Timing for the dedicated SFP+ control signals implemented in the transceiver are listed in Figure 6.

Application Support

An Evaluation Kit and Reference Designs are available to assist in evaluation of the AFBR-703SDDZ. Please contact your local Field Sales representative for availability and ordering details.

Caution

There are no user serviceable parts nor maintenance requirements for the AFBR-703SDDZ. All mechanical adjustments are made at the factory prior to shipment. Tampering with, modifying, misusing or improperly handling the AFBR-703SDDZ will void the product warranty. It may also result in improper operation and possibly overstress the laser source. Performance degradation or device failure may result. Connection of the AFBR-703SDDZ to a light source not compliant with IEEE Std. 802.3ae Clause 52 and SFF-8341 specifications, operating above maximum operating conditions or in a manner inconsistent with it's design and function may result in exposure to hazardous light radiation and may constitute an act of modifying or manufacturing a laser product. Persons performing such an act are required by law to recertify and re-identify the laser product under the provisions of U.S. 21 CFR (Subchapter J) and TUV.

Customer Manufacturing Processes

This module is pluggable and is not designed for aqueous wash, IR reflow, or wave soldering processes.

Ordering Information

Please contact your local field sales engineer or one of Avago Technologies franchised distributors for ordering information. For technical information, please visit Avago Technologies' WEB page at www.avagotech.com. For information related to SFF Committee documentation visit www.sffcommittee.org.

Regulatory Compliance

The AFBR-703SDDZ complies with all applicable laws and regulations as detailed in Table 1. Certification level is dependent on the overall configuration of the host equipment. The transceiver performance is offered as a figure of merit to assist the designer.

Electrostatic Discharge (ESD)

The AFBR-703SDDZ is compatible with ESD levels found in typical manufacturing and operating environments as described in Table 1. In the normal handling and operation of optical transceivers, ESD is of concern in two circumstances.

The first case is during handling of the transceiver prior to insertion into an SFP compliant cage. To protect the device, it's important to use normal ESD handling pre-cautions. These include use of grounded wrist straps, work-benches and floor wherever a transceiver is handled.

The second case to consider is static discharges to the exterior of the host equipment chassis after installation. If the optical interface is exposed to the exterior of host equipment cabinet, the transceiver may be subject to system level ESD requirements.

Electromagnetic Interference (EMI)

Equipment incorporating 10 gigabit transceivers is typically subject to regulation by the FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan. The AFBR-703SDDZ enables equipment compliance to these standards detailed in Table 1. The metal housing and shielded design of the AFBR-703SDDZ minimizes the EMI challenge facing the equipment designer. For superior EMI performance it is recommended that equipment designs utilize SFP+ cages per SFF 8432.

RF Immunity (Susceptibility)

Due to its proprietary bulk optics TOSA and ROSA design, the EMI immunity of the AFBR-703SDDZ exceeds typical industry standards.

Eye Safety

The AFBR-703SDDZ provides Class 1 (single fault tolerant) eye safety by design and has been tested for compliance with the requirements listed in Table 1. The eye safety circuit continuously monitors the optical output power level and will disable the transmitter upon detecting a condition beyond the scope of Class 1 certification Such conditions can be due to inputs from the host board (Vcc fluctuation, unbalanced code) or a fault within the transceiver. US CDRH and EU TUV certificates are listed in table 1.

Flammability

The AFBR-703SDDZ optical transceiver is made of metal and high strength, heat resistant, chemical resistant and UL 94V-0 flame retardant plastic.

Table 1. Regulatory Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Contacts	MIL-STD-883C Method 3015.4	Class 1 (> 2000 Volts)
Electrostatic Discharge (ESD) to the Duplex LC Receptacle	IEC 61000-4-2	Typically, no damage occurs with 25 kV when the duplex LC connector receptacle is contacted by a Human Body Model probe.
Life Traffic ESD Immunity	IEC 61000-4-2	10 contacts of 8 kV on the electrical faceplate with device inserted into a panel.
Life Traffic ESD Immunity	IEC 61000-4-2	Air discharge of 15 kV (min.) contact to connector without damage.
Electromagnetic Interference (EMI)	FCC Class B CENELEC EN55022 Class B (CISPR 22A) VCCI Class A	System margins are dependent on customer board and chassis design.
RF Immunity	IEC 61000-4-3	Typically shows no measurable effect from a 10 V/m field swept from 80MHz to 1 GHz
Laser Eye Safety and Equipment Type Testing TÜV Rheinland Product Safety BAUART GEPRÜFT TYPE APPROVED	US FDA CDRH AEL Class 1 US21 CFR, Subchapter J per Paragraphs 1002.10 and 1002.12 (IEC) EN60825-1: 1994 + A11 + A2 (IEC) EN60825-2: 1994 + A1 (IEC) EN60950: 1992 + A1 + A2 + A3 + A4 + A11	CDRH Accession No. 9720151-072 TUV File R 72071411 page 2
Component Recognition	Underwriters Laboratories and Canadian Standards Association Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment	UL file E173874
RoHS Compliance	RoHS Directive 2002/95/EC and it's amendment directives 6/6	SGS Test Report No. LPC/13392 (AD-1)/07 CTS Ref. CTS/07/3283/Avago

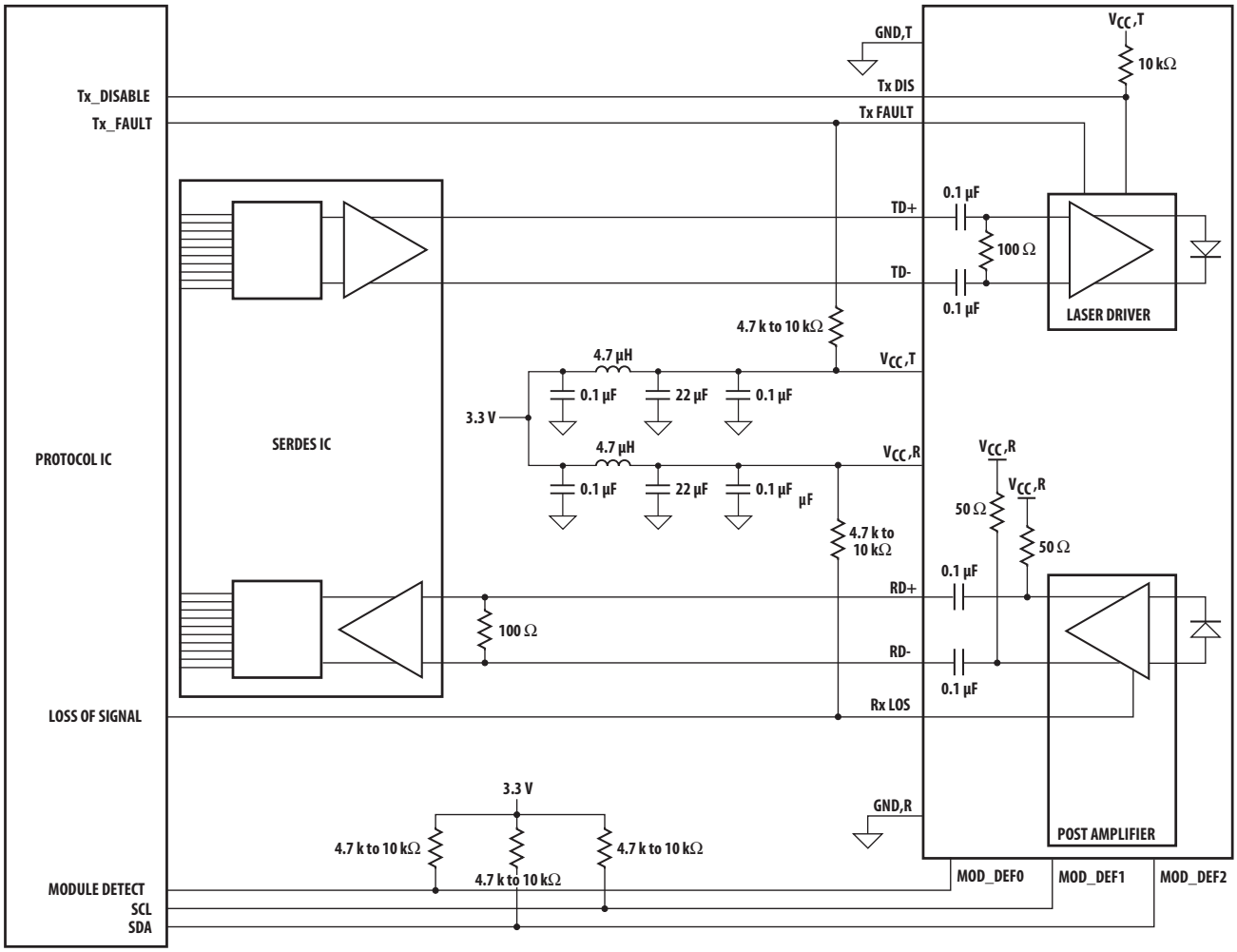
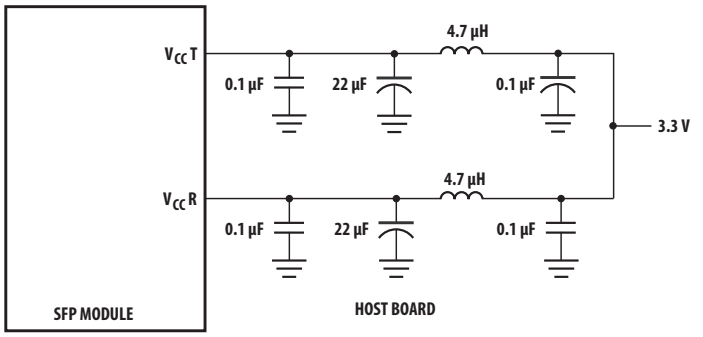


Figure 2. Typical application configuration.



NOTE: INDUCTORS MUST HAVE LESS THAN 1Ω SERIES RESISTANCE TO LIMIT VOLTAGE DROP TO THE SFP MODULE.

Figure 3. Recommended power supply filter.

Table 2. Contact Description

Contact	Symbol	Function/Description	Notes
1	VeeT	Transmitter Signal Ground	Note 1
2	TX_FAULT	Transmitter Fault (LVTTL-O) – High indicates a fault condition	Note 2
3	TX_DISABLE	Transmitter Disable (LVTTL-I) – High or open disables the transmitter	Note 3
4	SDA	Two Wire Serial Interface Data Line (LVCMOS – I/O) (same as MOD-DEF2 in INF-8074)	Note 4
5	SCL	Two Wire Serial Interface Clock Line (LVCMOS – I/O) (same as MOD-DEF1 in INF-8074)	Note 4
6	MOD_ABS	Module Absent (Output), connected to VeeT or VeeR in the module	Note 5
7	RS0	Rate Select 0 - RS0=Lo for 1000BASE-SX, RS0=Hi for 10GBASE-SR	Note 6
8	RX_LOS	Receiver Loss of Signal (LVTTL-O)	Note 2
9	RS1	Rate Select 1 - RS1=Lo for 1000BASE-SX, RS1=Hi for 10GBASE-SR	Note 6
10	VeeR	Receiver Signal Ground	Note 1
11	VeeR	Receiver Signal Ground	Note 1
12	RD-	Receiver Data Out Inverted (CML-O)	
13	RD+	Receiver Data Out (CML-O)	
14	VeeR	Receiver Signal Ground	
15	VccR	Receiver Power + 3.3 V	
16	VccT	Transmitter Power + 3.3 V	
17	VeeT	Transmitter Signal Ground	Note 1
18	TD+	Transmitter Data In (CML-I)	
19	TD-	Transmitter Data In Inverted (CML-I)	
20	VeeT	Transmitter Signal Ground	Note 1

Notes:
1. The module signal grounds are isolated from the module case.
2. This is an open collector/drain output that on the host board requires a 4.7 kΩ to 10 kΩ pullup resistor to VccHost. See Figure 2.
3. This input is internally biased high with a 4.7 kΩ to 10 kΩ pullup resistor to VccT.
4. Two-Wire Serial interface clock and data lines require an external pullup resistor dependent on the capacitance load.
5. This is a ground return that on the host board requires a 4.7 kΩ to 10 kΩ pullup resistor to VccHost.
6. Refer to the Appendix for detailed operation of RS0 and RS1.

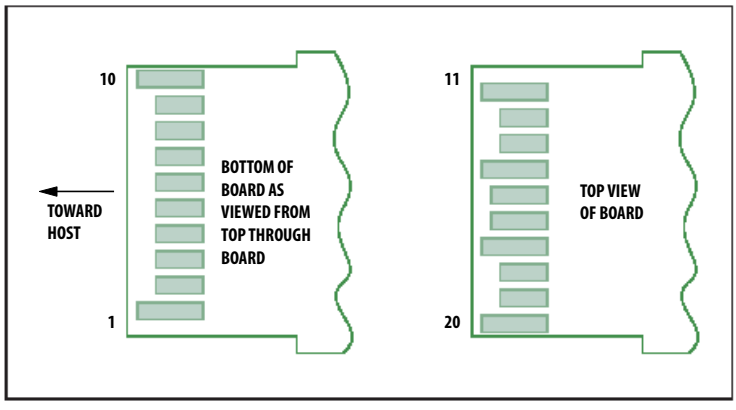


Figure 4. Module edge connector contacts

Table 3. Absolute Maximum Ratings

Stress in excess of any of the individual Absolute Maximum Ratings can cause immediate catastrophic damage to the module even if all other parameters are within Recommended Operating Conditions. It should not be assumed that limiting values of more than one parameter can be applied concurrently. Exposure to any of the Absolute Maximum Ratings for extended periods can adversely affect reliability.

Parameter	Symbol	Minimum	Maximum	Unit	Notes
Storage Temperature	T_S	-40	100	C	
Case Operating Temperature	T_C	-40	100	C	
Relative Humidity	RH	5	95	%	
Supply Voltage	VccT, VccR	-0.3	3.8	V	Note 1
Low Speed Input Voltage		-0.5	Vcc+0.5	V	
Two-Wire Interface Input Voltage		-0.5	Vcc+0.5	V	
High Speed Input Voltage, Single Ended		-0.3	Vcc+0.5	V	
High Speed Input Voltage, Differential			2.5	V	
Low Speed Output Current		-20	20	mA	
Optical Receiver Input Average Power			0	dBm	

Notes:
1. The module supply voltages, VccT and VccR must not differ by more than 0.5 V or damage to the device may occur.

Table 4. Recommended Operating Conditions

Recommended Operating Conditions specify parameters for which the electrical and optical characteristics hold unless otherwise noted. Optical and electrical charactristics are not defined for operation outside the Recommended Operating Conditions, reliability is not implied and damage to the module may occur for such operation over an extended period of time.

Parameter	Symbol	Minimum	Maximum	Unit	Notes
Case Operating Temperature	T_C	0	70	°C	Note 1
Module Supply Voltage	VccT, VccR	3.135	3.465	V	Fig. 3
Host Supply Voltage	VccHost	3.14	3.46	V	
Signal Rate 1000BASE-SX (1.25GBd Typical)		10.311	10.313	GBd	Note 2
Power Supply Noise Tolerance		66	10Hz to 10MHz	mVp-p	Fig. 3
Tx Input Single Ended DC Voltage Tolerance (Ref VeeT)	V	-0.3	4.0	V	
Rx Output Single Ended Voltage Tolerance	V	-0.3	4.0	V	

Notes:
1. Ambient operating temperature limits are based on the Case Operating Temperature limits and are subject to the host system thermal design. See Figure 7 for the module Tc reference point.
2. For 10GBASE-SR

Table 5. Low Speed Signal Electrical Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for Tc = 40°C. VccT and VccR = 3.3 V.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Module Supply Current	I_{CC}		180	289	mA	Note 1
Power Dissipation	P_{DISS}		600	1000	mW	
TX_FAULT, RX_LOS	I_{OH}	- 50		+ 37.5	µA	Note 2
	V_{OL}	- 0.3		0.4	V	
TX_DISABLE	V_{IH}	2.0		VccT + 0.3	V	Note 3
	V_{IL}	-0.3		0.8	V	

Notes:
1. Supply current includes both VccT and VccR connections.
2. Measured with a 4.7 kΩ load to VccHost.
3. TX_DISABLE has an internal 4.7 kΩ to 10 kΩ pull-up to VccT

Table 6. High Speed Signal Electrical Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for Tc = 40°C. VccT and VccR = 3.3 V.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Tx Input Differential Voltage (TD +/-)	V_I	180		1200	mVpp	Note 1
Tx Input AC Common Mode Voltage Tolerance				15	mV(RMS)	
Tx Input Differential S-parameter (100 Ω Ref.)	SDD11			Note 3	dB	0.01-11.1GHz
Tx Input Differential to Common Mode Conversion (25 Ω Ref.)	SCD11			-10	dB	0.01-11.1 GHz
Rx Output Differential Voltage (RD +/-)	Vo	300		850	mVpp	Note 1, 10 GBd 1.25 Gbd
Rx Output Termination Mismatch @ 1MHz	ΔZ_m			5	%	
Rx Output AC Common Mode Voltage				7.5	mV(RMS)	Note 5
Rx Output Output Rise and Fall Time (20% to 80%)	tr, tf	28			ps	
Rx Output Total Jitter	TJ			0.70 0.332	Ulp-p Ulp-p	Note 6, 10 GBd 1.25 Gbd
Rx Output 99% Jitter	DJ			0.42	Ulp-p	Note 6
Rx Output Differential S-parameter (100 Ω Ref.)	SDD22			Note 4	dB	0.01-11.1GHz
Rx Output Common Mode Reflection Coefficient (25 Ω Ref.)	SCC22			-6 -3	dB dB	0.01-2.5 GHz 2.5-11.1 GHz
Receiver Output Eye Mask						See Figure 5a

Notes:
1. Internally AC coupled and terminated (100 Ohm differential).
2. Internally AC coupled but requires an external load termination (100 Ohm differential).
3. Maximum reflection coefficient is expressed as SDD11=Max(-12+2*sqrt(f) , -6.3+13*log10(f/5.5)), for f in GHz.
4. Maximum reflection coefficient is expressed as SDD22=Max(-12+2*sqrt(f) , -6.3+13*log10(f/5.5)), for f in GHz.
5. The RMS value is measured by calculating the standard deviation of the histogram for one UI of the common mode signal.
6. TJ conditions per SFF-8431.

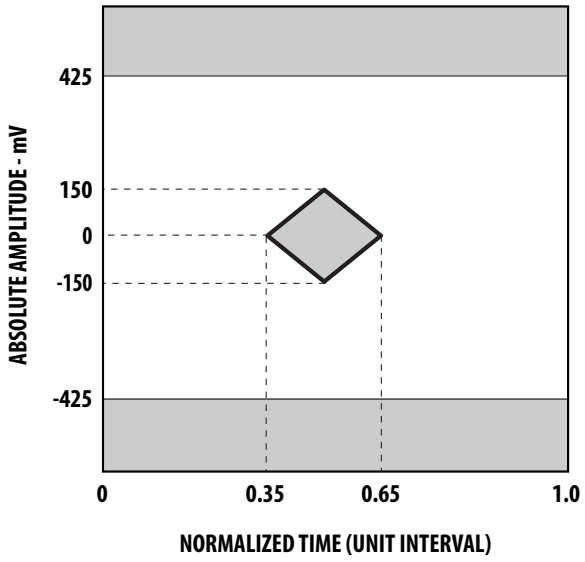


Figure 5a. 10GBd Receiver Electrical Optical Eye Mask Definition

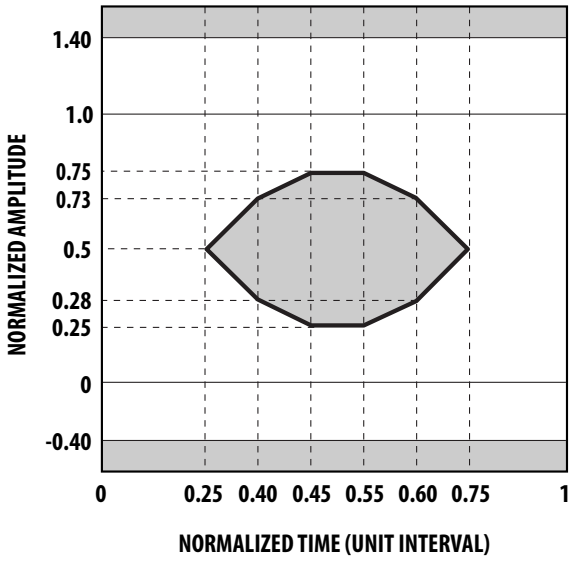


Figure 5b. 10GBd Transmitter Optical Eye Mask Definition

Table 7. Two-Wire Interface Electrical Characteristics

Parameter	Symbol	Min.	Max.	Unit	Conditions
Host Vcc Range	VccHTWI	3.135	3.465	V	
SCL and SDA	V_{OL}	0.0	0.40	V	Rp[1] pulled to VccHTWI, measured at host side of connector
	V_{OH}	VccHTWI - 0.5	VccHTWI + 0.3	V	
SCL and SDA	V_{IL}	-0.3	VccT*0.3	V	
	V_{IH}	VccT*0.7	VccT + 0.5	V	
Input Current on the SCL and SDA Contacts	I_I	-10	10	µA	
Capacitance on SCL and SDA Contacts	C_i[2]		14	pF	
Total bus capacitance for SCL and for SDA	C_b[3]		100	pF	At 400 kHz, 3.0 kΩ Rp, max At 100 kHz, 8.0 kΩ Rp, max
			290	pF	At 400 kHz, 1.1 kΩ Rp, max At 100 kHz, 2.75 kΩ Rp, max

Notes:
1. Rp is the pull up resistor. Active bus termination may be used by the host in place of a pullup resistor. Pull ups can be connected to various power supplies, however the host board design shall ensure that no module contact has voltage exceeding VccT or VccR by 0.5 V nor requires the module to sink more than 3.0 mA current.
2. C_i is the capacitance looking into the module SCL and SDA contacts
3. C_b is the total bus capacitance on the SCL or SDA bus.

Table 8a. 10GBd Optical Specifications - Transmitter

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for Tc = 40°C. VccT and VccR = 3.3 V.

Parameter	Minimum	Typical	Maximum	Units	Notes
Laser OMA output power	-4.3			dBm	1, 2, 3, See Table 9
Laser mean output power			-1.0	dBm	1, 2, 4
Laser off power			-30	dBm	1
Extinction ratio	3.0			dB	1, 2
Transmitter and dispersion penalty (TDP)			3.9	dB	1
Center Wavelength	840		860	nm	1,3, See Table 9
RMS spectral width, standard deviation					1,3, See Table 9
$RIN_{12}OMA$			-128	dB/Hz	1
Optical Return Loss Tolerance			12	dB	1
Encircled Flux					5
Transmitter Output Eye Mask					1, See Figure 5b

General Specification Considerations (Notes):

1. IEEE 802.3ae Clause 52 compliant.
2. These parameters are interrelated: see IEEE 802.3ae, Clause 52.
3. See Table 9. Trade-offs are available among spectral width, center wavelength, and minimum optical modulation amplitude.
4. The 10GBASE-SR launch power shall be the lesser of the Class 1 safety limit as defined in IEEE 802.3ae 52.10.2 or the average receive power maximum defined by IEEE 802.3ae -2002 Table 52-9.
5. The transceiver's launch condition meets the requirement of 10 Gigabit Ethernet multimode fiber as detailed in TIA 492AAAC.
6. Vertical eye closure penalty and Stressed eye jitter are test conditions for Stressed sensitivity (OMA) measurements.

Table 8b. 1.25GBd Optical Characteristics - Transmitter

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Output Optical Power (Average)	P_{OUT}	-9.5	-6.5	-1	dBm	1
Optical Extinction Ratio	ER	9	12		dB	
Total Jitter (TP1 to TP2 Contribution	TJ			227	ps	
				0.284	UI	
Coupled Power Ratio	CPR	9			dB	

Notes:

1. 50/125 µm fiber with NA = 0.2, 62.5/125 µm fiber with NA = 0.275.

Table 9a. 10GBd Optical Specifications - Receiver

Parameter	Minimum	Typical	Maximum	Units	Notes
Stressed sensitivity (OMA)	–		-7.5	dBm	1
Receive sensitivity (OMA)			-11.1	dBm	
Receive Power (P_{ave}) Overload	-1.0			dBm	1
Reflectance			-12	dB	1
Center Wavelength	840		860	nm	1
RX_LOS (OMA) De-Asserted			-12	dBm	
RX_LOS (OMA) Asserted	-30			dBm	
RX_LOS (OMA) Hysteresis	0.5			dB	
Vertical eye closure penalty	3.5			dB	6
Stressed eye jitter	0.3			UI p-p	6
Electrical 3dB Cutoff Frequency			12.3	GHz	

General Specification Considerations (Notes):

1. IEEE 802.3ae Clause 52 compliant.
2. These parameters are interrelated: see IEEE 802.3ae, Clause 52.
3. See Table 9. Trade-offs are available among spectral width, center wavelength, and minimum optical modulation amplitude.
4. The 10GBASE-SR launch power shall be the lesser of the Class 1 safety limit as defined in IEEE 802.3ae 52.10.2 or the average receive power maximum defined by IEEE 802.3ae -2002 Table 52-9.
5. The transceiver's launch condition meets the requirement of 10 Gigabit Ethernet multimode fiber as detailed in TIA 492AAAC.
6. Vertical eye closure penalty and Stressed eye jitter are test conditions for Stressed sensitivity (OMA) measurements.

Table 9b. 1.25GBd Optical Characteristics - Receiver

Parameter	Minimum	Typical	Maximum	Unit	Notes
Receiver Sensitivity (Optical Input Power)		-21	-17	dBm	
Stressed Receiver Sensitivity			-12.5	dBm	62.5/125 mm fiber
			-13.5	dBm	50/125 mm fiber
Total Jitter (TP3 to TP4 Contribution 1.25GBd)			266	ps	
			0.332	UI	
RX_LOS(OMA) De-Asserted	-		-17	dBm	
RX_LOS(OMA) Asserted	-30			dBm	
RX_LOS(OMA) Hysterisis		3		dB	
Receive Electrical 3 dB Upper Cutoff Frequency		2.5	4	GHz	
Average Receive Power			0	dBm	
Wavelength	770		860	nm	

Table 10. 10 GBd Minimum Optical Modulation Amplitude

Center Wavelength (nm)	RMS Spectral Width (nm)								
	Up to 0.05	0.05 to 0.1	0.1 to 0.15	0.15 to 0.2	0.2 to 0.25	0.25 to 0.3	0.3 to 0.35	0.35 to 0.4	0.4 to 0.45
840 to 842	-4.2	-4.2	-4.1	-4.1	-3.9	-3.8	-3.5	-3.2	-2.8
842 to 844	-4.2	-4.2	-4.2	-4.1	-3.9	-3.8	-3.6	-3.3	-2.9
844 to 846	-4.2	-4.2	-4.2	-4.1	-4.0	-3.8	-3.6	-3.3	-2.9
846 to 848	-4.3	-4.2	-4.2	-4.1	-4.0	-3.8	-3.6	-3.3	-2.9
848 to 850	-4.3	-4.2	-4.2	-4.1	-4.0	-3.8	-3.6	-3.3	-3.0
850 to 852	-4.3	-4.2	-4.2	-4.1	-4.0	-3.8	-3.6	-3.4	-3.0
852 to 854	-4.3	-4.2	-4.2	-4.1	-4.0	-3.9	-3.7	-3.4	-3.1
854 to 856	-4.3	-4.3	-4.2	-4.1	-4.0	-3.9	-3.7	-3.4	-3.1
856 to 858	-4.3	-4.3	-4.2	-4.1	-4.0	-3.9	-3.7	-3.5	-3.1
858 to 860	-4.3	-4.3	-4.2	-4.2	-4.1	-3.9	-3.7	-3.5	-3.2

Table 11. Control Functions: Low Speed Signals Timing Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Symbol	Minimum	Maximum	Unit	Notes
TX_DISABLE Assert Time	t_off		10	µs	Note 1 , Fig. 6
TX_DISABLE Negate Time	t_on		1	ms	Note 2 , Fig. 6
Time to initialize, including reset of TX_FAULT	t_init		300	ms	Note 3 , Fig. 6
TX_FAULT Assert Time	t_fault		100	µs	Note 4 , Fig. 6
TX_DISABLE to Reset	t_reset	10		µs	Note 5 , Fig. 6
RX_LOS Assert Time	t_los_on		100	µs	Note 6 , Fig. 6
RX_LOS Deassert Time	t_los_off		0	µs	Note 7 , Fig. 6
Rate select Time	t_rate		40	ms	

Notes:
1. Time from rising edge of TX_DISABLE to when the optical output falls below 10% of nominal. A 10 ms interval between assertions of TX_DISABLE is required.
2. Time from falling edge of TX_DISABLE to when the modulated optical output rises above 90% of nominal.
3. Time from power on or falling edge of TX_DISABLE to when the modulated optical output rises above 90% of nominal and the Two-Wire interface is available.
4. From power on or negation of TX_FAULT using TX_DISABLE.
5. Time TX_DISABLE must be held high to reset the laser fault shutdown circuitry.
6. Time from loss of optical signal to Rx_LOS Assertion.
7. Time from valid optical signal to Rx_LOS De-Assertion.

Table 12. Control Functions: Two-Wire Interface Timing Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted.

Parameter	Symbol	Minimum	Maximum	Unit	Notes
TX_DISABLE Assert Time	t_off_twi		100	ms	Note 1
TX_DISABLE Negate Time	t_on_twi		100	ms	Note 2
TX_FAULT Assert Time	t_fault_twi		100	ms	Note 3
Rx_LOS Assert Time	t_loss_on_twi		100	ms	Note 4
Rx_LOS Deassert Time	t_loss_off_twi		100	ms	Note 5
Analog parameter data ready	t_data		1000	ms	Note 6
Two-Wire Interface Ready	t_serial		300	ms	Note 7
Write Cycle Time Parameter	t_write		80	ms	Note 8
Two-Wire Interface Clock Rate	f_serial_clock		400	kHz	
Time bus free before new transmission can start	t_buf	20		µs	Note 9

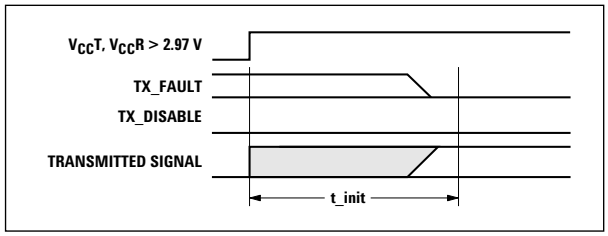
Notes:

1. Time from two-wire interface assertion of TX_DISABLE (A2h, byte 110, bit 6) to when the optical output falls below 10% of nominal. Measured from falling clock edge after stop bit of write transaction.
2. Time from two-wire interface de-assertion of TX_DISABLE (A2h, byte 110, bit 6) to when the modulated optical output rises above 90% of nominal.
3. Time from fault to two-wire interface TX_FAULT (A2h, byte 110, bit 2) asserted.
4. Time for two-wire interface assertion of Rx_LOS (A2h, byte 110, bit 1) from loss of optical signal.
5. Time for two-wire interface de-assertion of Rx_LOS (A2h, byte 110, bit 1) from presence of valid optical signal.
6. From power on to data ready bit asserted (A2h, byte 110, bit 0). Data ready indicates analog monitoring circuitry is functional.
7. Time from power on until module is ready for data transmission over the two-wire interface (reads or writes over A0h and A2h).
8. Time from stop bit to completion of a 1-8 byte write command. Measured from the stop bit, for a one t om four byte write the maximum cycle time is 40ms and for a five to eight byte write the maximum cycle time is 80ms.
9. Between STOP and START. See SFF 8431 Section 4.3

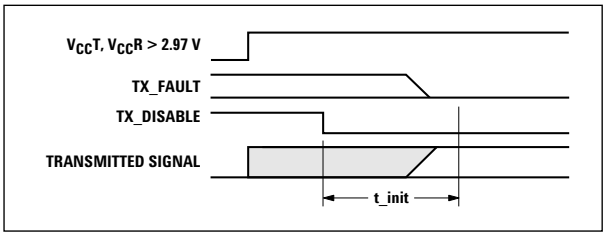
Table 13. Transceiver Digital Diagnostic Monitor (Real Time Sense) Characteristics

The following characteristics are defined over the Recommended Operating Conditions unless otherwise noted. Typical values are for Tc = 40°C. VccT and VccR = 3.3 V.

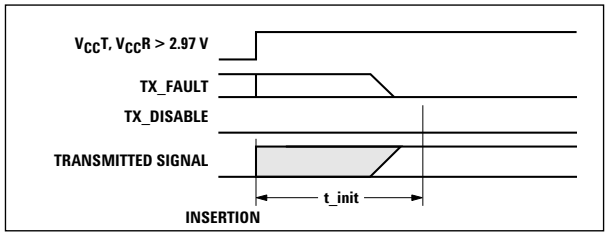
Parameter	Symbol	Min.	Units	Notes
Transceiver Internal Temperature Accuracy	T_{INT}	±3.0	°C	Temperature is measured internal to the transceiver. Valid from = -10°C to 85°C case temperature.
Transceiver Internal Supply Voltage Accuracy	V_{INT}	±0.1	V	Supply voltage is measured internal to the transceiver and can, with less accuracy, be correlated to voltage at the VccT contact. Valid over 3.3 V ± 10%.
Transmitter Laser DC Bias Current Accuracy	I_{INT}	±10	%	I_{INT} accuracy is better than ±10% of the nominal value.
Transmitted Average Optical Output Power Accuracy	P_T	±3.0	dB	Average Power coupled into 50/125 µm multi-mode fiber. Valid from100 µW to 500 µW.
Received Average Optical Input Power Accuracy	P_R	±3.0	dB	Average Power coupled from 50/125 µm multi-mode fiber. Valid from 77 µW to 500 µW.



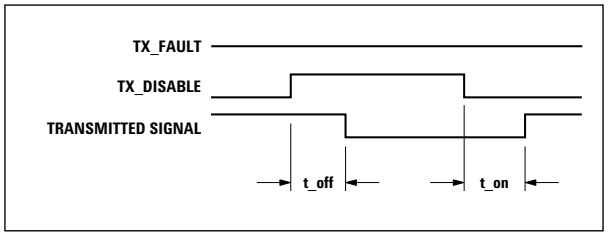
t-init: TX DISABLE NEGATED



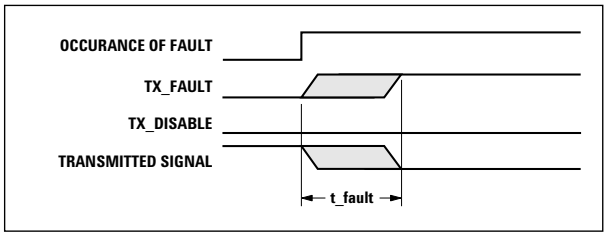
t-init: TX DISABLE ASSERTED



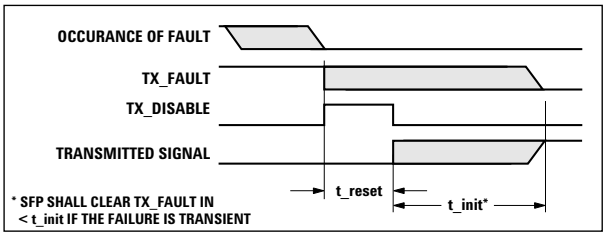
t-init: TX DISABLE NEGATED, MODULE HOT PLUGGED



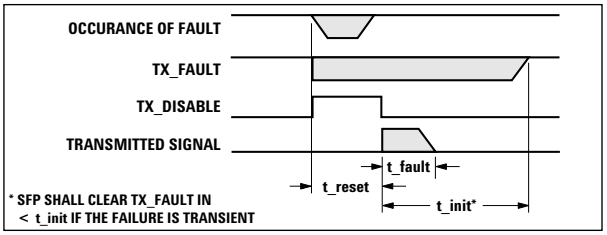
t-off & t-on: TX DISABLE ASSERTED THEN NEGATED



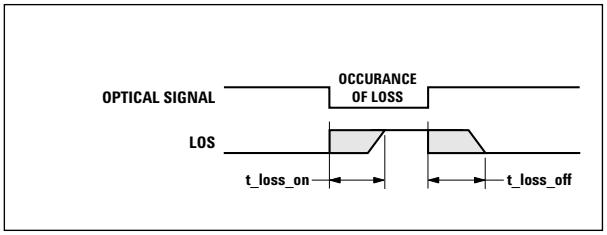
t-fault: TX FAULT ASSERTED, TX SIGNAL NOT RECOVERED



t-reset: TX DISABLE ASSERTED THEN NEGATED, TX SIGNAL RECOVERED



t-fault: TX DISABLE ASSERTED THEN NEGATED, TX SIGNAL NOT RECOVERED



t-los-on & t-los-off

Figure 6. Transceiver timing diagrams (module installed and power applied except where noted)

Table 14. EEPROM Serial ID Memory Contents – Conventional SFP Memory (Address A0h)

Byte # Decimal	Data Hex	Notes	Byte # Decimal	Data Hex	Notes
0	03	SFP physical device	37	00	Hex Byte of Vendor OUI[1]
1	04	SFP function defined by serial ID only	38	17	Hex Byte of Vendor OUI[1]
2	07	LC optical connector	39	6A	Hex Byte of Vendor OUI[1]
3	10	10G BASE-SR	40	41	"A" - Vendor Part Number ASCII character
4	00		41	46	"F" - Vendor Part Number ASCII character
5	00		42	42	"B" - Vendor Part Number ASCII character
6	01		43	52	"R" - Vendor Part Number ASCII character
7	00		44	2D	"-" - Vendor Part Number ASCII character
8	00		45	37	"7" - Vendor Part Number ASCII character
9	00		46	30	"0" - Vendor Part Number ASCII character
10	00		47	33	"3" - Vendor Part Number ASCII character
11	06	64B/66B	48	53	"S" - Vendor Part Number ASCII character
12	67	10312.5 Mbit/sec nominal bit rate (10.3125 Gbit/s)	49	44	"D" - Vendor Part Number ASCII character
13	00	Unspecified	50	44	"D" - Vendor Part Number ASCII character
14	00		51	5A	"Z" - Vendor Part Number ASCII character
15	00		52	20	" " - Vendor Part Number ASCII character
16	08	82 m of OM2 50/125 µm fiber	53	20	" " - Vendor Part Number ASCII character
17	03	33 m of OM1 62.5/125 µm fiber	54	20	" " - Vendor Part Number ASCII character
18	00		55	20	" " - Vendor Part Number ASCII character
19	1E	300 m of OM3 50/125 µm fiber	56	20	" " - Vendor Revision Number ASCII character
20	41	"A" - Vendor Name ASCII character	57	20	" " - Vendor Revision Number ASCII character
21	56	"V" - Vendor Name ASCII character	58	20	" " - Vendor Revision Number ASCII character
22	41	"A" - Vendor Name ASCII character	59	20	" " - Vendor Revision Number ASCII character
23	47	"G" - Vendor Name ASCII character	60	03	Hex Byte of Laser Wavelength[2]
24	4F	"O" - Vendor Name ASCII character	61	52	Hex Byte of Laser Wavelength[2]
25	20	" " - Vendor Name ASCII character	62	00	
26	20	" " - Vendor Name ASCII character	63		Checksum for Bytes 0-62[3]
27	20	" " - Vendor Name ASCII character	64	00	Receiver limiting output. 1 Watt power class.
28	20	" " - Vendor Name ASCII character	65	3A	Hardware SFP TX_DISABLE, TX_FAULT, & RX_LOS, RATE_SELECT
29	20	" " - Vendor Name ASCII character	66	00	
30	20	" " - Vendor Name ASCII character	67	00	
31	20	" " - Vendor Name ASCII character	68-83		Vendor Serial Number ASCII characters[4]
32	20	" " - Vendor Name ASCII character	84-91		Vendor Date Code ASCII characters[5]
33	20	" " - Vendor Name ASCII character	92	68	Digital Diagnostics, Internal Cal, Rx Pwr Avg
34	20	" " - Vendor Name ASCII character	93	FA	A/W, Soft SFP TX_DISABLE, TX_FAULT, & RX_LOS, RATE_SELECT
35	20	" " - Vendor Name ASCII character	94	03	SFF-8472 Compliance to revision 10.0
36	00		95		Checksum for Bytes 64-94[3]
			96 - 255	00	

Notes:
1. The IEEE Organizationally Unique Identifier (OUI) assigned to Avago Technologies is 00-17-6A (3 bytes of hex).
2. Laser wavelength is represented in 16 unsigned bits. The hex representation of 850 (nm) is 0352.
3. Addresses 63 and 95 are checksums calculated (per SFF-8472) and stored prior to product shipment.
4. Addresses 68-83 specify the AFBR-703SDDZ ASCII serial number and will vary on a per unit basis.
5. Addresses 84-91 specify the AFBR-703SDDZ ASCII date code and will vary on a per date code basis.

Table 15. EEPROM Serial ID Memory Contents – Enhanced Feature Set Memory (Address A2h)

Byte # Decimal	Notes	Byte # Decimal	Notes	Byte # Decimal	Notes
0	Temp H Alarm MSB [1]	26	Tx Pwr L Alarm MSB [4]	104	Real Time Rx Pwr MSB [5]
1	Temp H Alarm LSB [1]	27	Tx Pwr L Alarm LSB [4]	105	Real Time Rx Pwr LSB [5]
2	Temp L Alarm MSB [1]	28	Tx Pwr H Warning MSB [4]	106	Reserved
3	Temp L Alarm LSB [1]	29	Tx Pwr H Warning LSB [4]	107	Reserved
4	Temp H Warning MSB [1]	30	Tx Pwr L Warning MSB [4]	108	Reserved
5	Temp H Warning LSB [1]	31	Tx Pwr L Warning LSB [4]	109	Reserved
6	Temp L Warning MSB [1]	32	Rx Pwr H Alarm MSB [5]	110	Status/Control - See Table 17
7	Temp L Warning LSB [1]	33	Rx Pwr H Alarm LSB [5]	111	Reserved
8	Vcc H Alarm MSB [2]	34	Rx Pwr L Alarm MSB [5]	112	Flag Bits - See Table 18
9	Vcc H Alarm LSB [2]	35	Rx Pwr L Alarm LSB [5]	113	Flag Bits - See Table 18
10	Vcc L Alarm MSB [2]	36	Rx Pwr H Warning MSB [5]	114	Reserved
11	Vcc L Alarm LSB [2]	37	Rx Pwr H Warning LSB [5]	115	Reserved
12	Vcc H Warning MSB [2]	38	Rx Pwr L Warning MSB [5]	116	Flag Bits - See Table 18
13	Vcc H Warning LSB [2]	39	Rx Pwr L Warning LSB [5]	117	Flag Bits - See Table 18
14	Vcc L Warning MSB [2]	40-55	Reserved	118	Extended Control/Status byte - See Table 16
15	Vcc L Warning LSB [2]	56-94	External Calibration Constants [6]	119-127	Reserved
16	Tx Bias H Alarm MSB [3]	95	Checksum for Bytes 0-94 [7]	128-247	Customer Writeable
17	Tx Bias H Alarm LSB [3]	96	Real Time Temperature MSB [1]	248-255	Vendor Specific
18	Tx Bias L Alarm MSB [3]	97	Real Time Temperature LSB [1]		
19	Tx Bias L Alarm LSB [3]	98	Real Time Vcc MSB [2]		
20	Tx Bias H Warning MSB [3]	99	Real Time Vcc LS [2]		
21	Tx Bias H Warning LSB [3]	100	Real Time Tx Bias MSB [3]		
22	Tx Bias L Warning MSB [3]	101	Real Time Tx Bias LSB [3]		
23	Tx Bias L Warning LSB [3]	102	Real Time Tx Power MSB [4]		
24	Tx Pwr H Alarm MSB [4]	103	Real Time Tx Power LSB [4]		
25	Tx Pwr H Alarm LSB [4]				

Notes:
1. Temperature (Temp) is decoded as a 16 bit signed twos compliment integer in increments of 1/256°C.
2. Supply Voltage (Vcc) is decoded as a 16 bit unsigned integer in increments of 100 μV.
3. Laser bias current (Tx Bias) is decoded as a 16 bit unsigned integer in increments of 2 μA.
4. Transmitted average optical power (Tx Pwr) is decoded as a 16 bit unsigned integer in increments of 0.1 μW.
5. Received average optical power (Rx Pwr) is decoded as a 16 bit unsigned integer in increments of 0.1 μW.
6. Bytes 56-94 are not intended for use with AFBR-703SDDZ, but have been set to default values per SFF-8472.
7. Byte 95 is a checksum calculated (per SFF-8472) and stored prior to product shipment.
8. See Table 16.

Table 16. EEPROM Serial ID Memory Contents - Extended Control/Status (Address A2h, Byte 118)

Bit #	Status/ Control Name	Description	Notes
7	Reserved		
6	Reserved		
5	Reserved		
4	Reserved		
3	Soft RS1 Select	Read/write bit that allows software Tx rate control. Writing '1' selects full lspeed Tx operation. Power on default is logic zero/low. This bit is OR'd with the hardware RS1 pin value (see Appendix).	1
2	Reserved		
1	Class2 Operation State	Value=0. Power class2 operation is not active.	
0	Power Class Select	Has no effect.	

Notes:
1. The response time for soft commands of the AFBR-703SDDZ is 100ms as specified by SFF-8472.

Table 17. EEPROM Serial ID Memory Contents – Soft Commands (Address A2h, Byte 110)

Bit #	Status/ Control Name	Description	Notes
7	TX_ DISABLE State	Digital state of SFP TX_ DISABLE Input (1 = TX_DISABLE asserted)	Note 1
6	Soft TX_ DISABLE	Read/write bit for changing digital state of TX_DISABLE function	Note 1, 2
5	Reserved		
4	Reserved		
3	Soft RS0 Select	Read/write bit that allows software RX rate control. Writing '1' selects full speed RX operation. Power on default is logic zero/low. This bit is OR'd with the hardware RS0 pin value (see Appendix).	
2	TX_FAULT State	Digital state of the SFP TX_FAULT Output (1 = TX_FAULT asserted)	Note 1
1	RX_LOS State	Digital state of the SFP RX_LOS Output (1 = RX_LOS asserted)	Note 1
0	Data Ready (Bar)	Indicates transceiver is powered and real time sense data is ready. (0 = Ready)	

Notes:
1. The response time for soft commands of the AFBR-703SDDZ is 100 msec as specified by SFF-8472.
2. Bit 6 is logic OR'd with the SFP TX_DISABLE input on contact 3; either asserted will disable the SFP+ transmitter.

Table 18. EEPROM Serial ID Memory Contents – Alarms and Warnings (Address A2h, Bytes 112, 113, 116, 117)

Byte	Bit	Flag Bit Name Description	
112	7	Temp High Alarm	Set when transceiver internal temperature exceeds high alarm threshold
	6	Temp Low Alarm	Set when transceiver internal temperature exceeds low alarm threshold
	5	Vcc High Alarm	Set when transceiver internal supply voltage exceeds high alarm threshold
	4	Vcc Low Alarm	Set when transceiver internal supply voltage exceeds low alarm threshold
	3	Tx Bias High Alarm	Set when transceiver laser bias current exceeds high alarm threshold
	2	Tx Bias Low Alarm	Set when transceiver laser bias current exceeds low alarm threshold
	1	Tx Power High Alarm	Set when transmitted average optical power exceeds high alarm threshold
	0	Tx Power Low Alarm	Set when transmitted average optical power exceeds low alarm threshold
113	7	Rx Power High Alarm	Set when received average optical power exceeds high alarm threshold
	6	Rx Power Low Alarm	Set when received average optical power exceeds low alarm threshold
	0-5	Reserved	
116	7	Temp High Warning	Set when transceiver internal temperature exceeds high warning threshold
	6	Temp Low Warning	Set when transceiver internal temperature exceeds low warning threshold
	5	Vcc High Warning	Set when transceiver internal supply voltage exceeds high warning threshold
	4	Vcc Low Warning	Set when transceiver internal supply voltage exceeds low warning threshold
	3	Tx Bias High Warning	Set when transceiver laser bias current exceeds high warning threshold
	2	Tx Bias Low Warning	Set when transceiver laser bias current exceeds low warning threshold
	1	Tx Power High Warning	Set when transmitted average optical power exceeds high warning threshold
	0	Tx Power Low Warning	Set when transmitted average optical power exceeds low warning threshold
117	7	Rx Power High Warning	Set when received average optical power exceeds high warning threshold
	6	Rx Power Low Warning	Set when received average optical power exceeds low warning threshold
	0-5	Reserved	

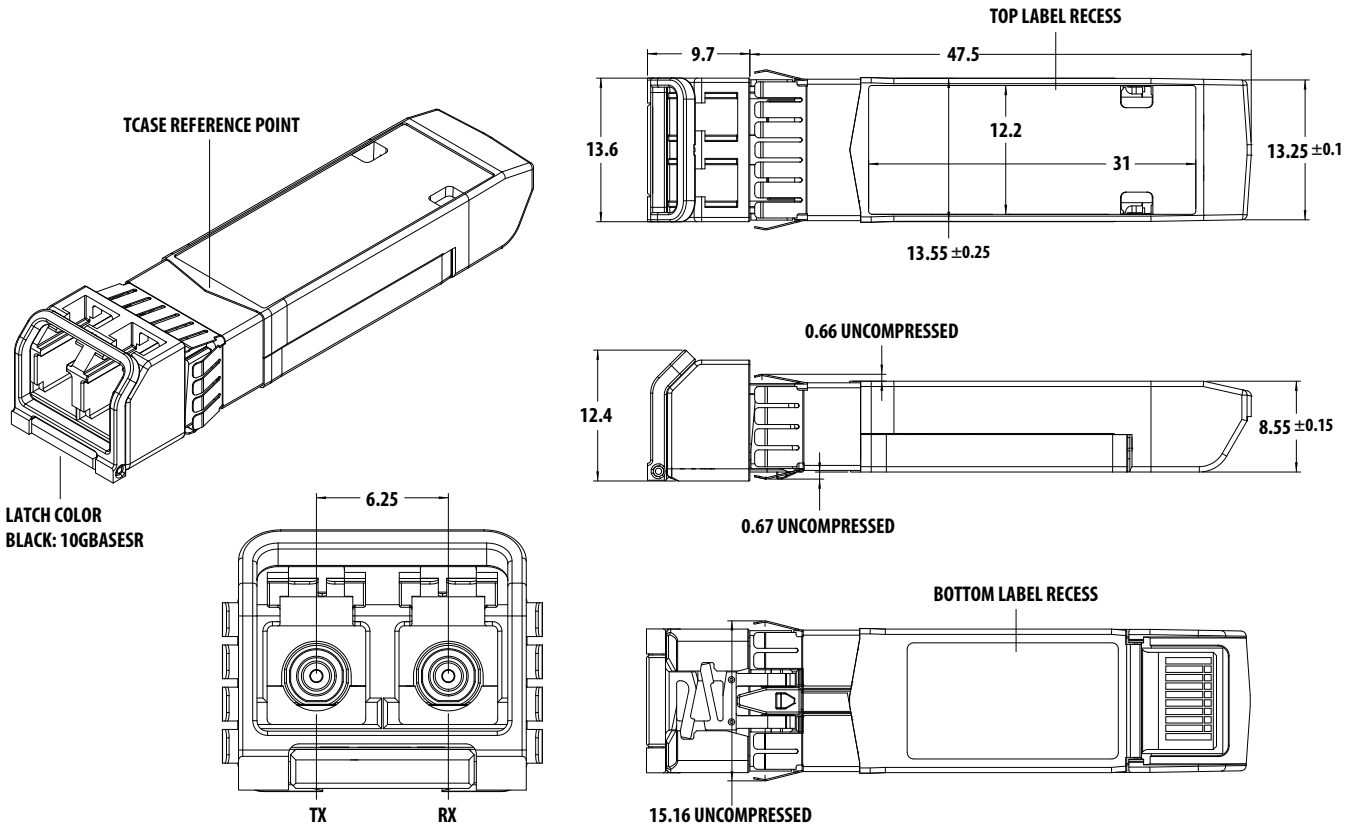


Figure 7. Module Drawing

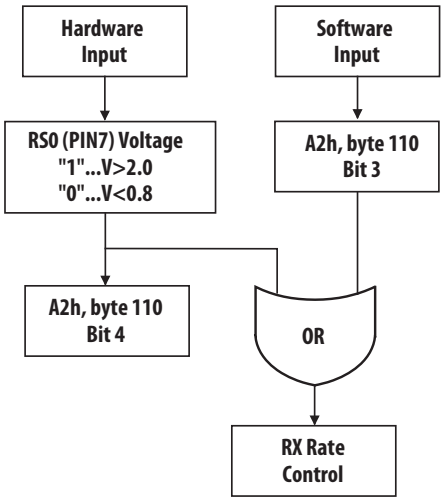


Figure 8. Module label

Appendix: Rate Select Control

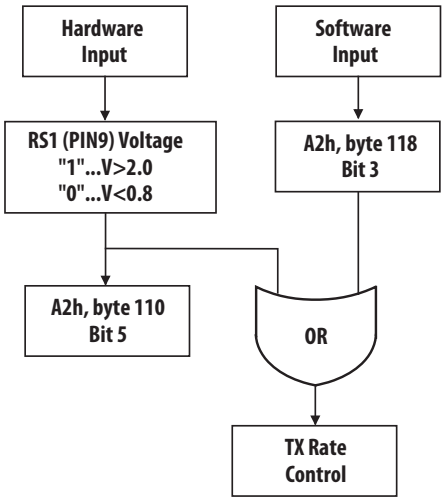
RX and TX rates can be independently controlled by either hardware input pins or via register writes. Module electrical input pins 7 and 9 are used to select RX and TX rate respectively. Status of each logic level is reflected to register byte 110 bit 4 and 5 on address A2h as shown in the diagram below. RX and TX rates can also be controlled by register writes to byte 110 bit 3 and 118 bit 3. Power on default of these bits are logic low. Hardware and software control inputs are OR'd to allow flexible control.

RS0 RX Rate Select control flow



RS0 Control Input		RX Operation
Hardware	Software	
0	0	1.25G
0	1	10G
1	0	10G
1	1	10G

RS1 TX Rate Select control flow



RS1 Control Input		TX Operation
Hardware	Software	
0	0	1.25G
0	1	10G
1	0	10G
1	1	10G

For product information and a complete list of distributors, please go to our website: **www.avagotech.com**

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AV02-1967EN - January 28, 2013